



LEGIC 6000 series

General Information

SM-63x0 EMS Manufacturer Information

CONFIDENTIAL

Classification: Public (Info Level 1)

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1 About this document

Scope This document provides hardware information of the LEGIC 6000 series reader chips SM-63x0 with hardware versions V1.1 and V1.2 and with LEGIC OS50. This document includes information relevant for electronics manufacturing services.

Target users This document is aimed at hardware and software engineers of electronics manufacturing services (EMS).

Terms and abbreviations The following table lists only terms and abbreviations used exclusively in this document:

Term	Description
SM-63x0	Abbreviation for any 6000 series reader chip type (SM-6300, SM-6300 <i>init</i> , SM-6310 and SM-6310 <i>init</i>)

Table 1: Terms and abbreviations

Document conventions

Description	Example
Notes and examples appear in italics	<i>Note</i>
Commands appear in capital letters	SEARCH
Hexadecimal figures appear in the form 0xnm	0x23
Code snippets appear in monospace font	// PARAMETER
User input appear in monospace font	Enter phone#+410765678899.
GUI elements appear in bold font	Click Create .
New or important terms appear in bold font	APPL_STATE [Reset]: A hardware reset is executed after the answer has been sent and all volatile keys are lost.

Table 2: Typographical conventions



This symbol marks warnings and important passages.

1.1 Change history

Latest changes	Change	Edition	Doc. No.
	Chapter 2: Technical data: Details about 'Current chip designation' added.	04.2023	LR6-22-101d

Table 3: Latest changes

Change history	Change	Edition	Doc. No.
	Entire document: Minor text changes to improve comprehensibility.	12.2021	LR6-22-101c
	Chapter 2: Technical data: Illustration 1 'Chip designation prior to 01.01.2020' added. Breakdown between SM-6300 and SM-6310 explained and Notes adjusted.		
	Chapter 3: Processing: Information about moisture sensitivity added, Illustration 9 'MSL label' and table 8 'Bake parameter' added.		
	Entire document: Minor text changes to improve comprehensibility.	09.2020	LR6-22-101b
	First edition	09.2020	LR6-22-101a

Table 4: Change history

2 Technical data

Current chip designation (01.2020 - present)

Pin 1 Designator →

Product Name* → SM-6300

Hardware Version → V15 M5LLLLY ←

V = Version
1st Digit = Main Version
2nd Digit = Minor Version

M = Month
5 = Code for Factory Use
LLLL = Lot Information
Y = Year

Legend: * SM-6300 and SM-6310 are both marked as SM-6300

Code M breakdown

Code	A	B	C	D	E	F	G	H	J	K	L	M
Month	Jan.	Feb.	Mar.	Apr.	May	June	July	Aug.	Sept.	Oct.	Nov.	Dec.

Code Y breakdown

Code	V	A	B	C	D	E	F	G	H	J
Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029

Examples:

Hardware version V15 to be interpreted as Version 1.5

Date Code A50013V to be interpreted as January 2020, Lot Nr.0013

Former chip designation (earlier than 2020)

Pin 1 Designator →

Product Name* → SM-6300

Hardware Version → V12 YYMMLLL ←

V = Version
1st Digit = Main Version
2nd Digit = Minor Version

YY = Year
MM = Month
LLL = Lot Information

Legend: * SM-6300 and SM-6310 are both marked as SM-6300

Code YY breakdown

Code	17	18	19	20
Year	2017	2018	2019	2020

Code MM breakdown

Code	01	02	03	04	05	06	07	08	09	10	11	12
Month	Jan.	Feb.	Mar.	Apr.	May	June	July	Aug.	Sept.	Oct.	Nov.	Dec.

Examples:

Hardware version V12 to be interpreted as Version 1.2

Date Code 1702013 to be interpreted as February 2017, Lot Nr.0013

- Notes**
- The product name can be read with the `GET_IDB [VERSIONS]` command.
 - 0x04 = SM-6300
 - 0x05 = SM-6310
 - The firmware version (LEGIC OS50) can be read with the `GET_IDB [VERSIONS]` command. Example: 0x01 07 03 00 = V1.7.3.0
 - The Security Modules are delivered on tape.

Ambient conditions

Designation	Min.	Typ.	Max.	Conditions
Operation				
Ambient temperature	-40 °C	25 °C	85 °C	
Junction temperature			110 °C	
Thermal resistance		29.7 °C/W		Junction to case
Power dissipation double supply		865 mW*		'RF on' state, VCC = 5 V, I = 173 mA
Power dissipation single supply		330 mW**		'RF on' state, VCC = 3.3 V, I = 112 mA
Power dissipation digital supply		46 mW		DVCC = 3.3 V, 14 mA
Storage, transport				
Ambient temperature	-40 °C		105 °C	

Table 5: Ambient conditions

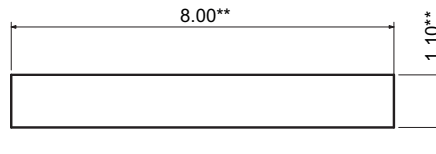
Legend: * 345 mW emitted by antenna
 ** 125 mW emitted by antenna

Package

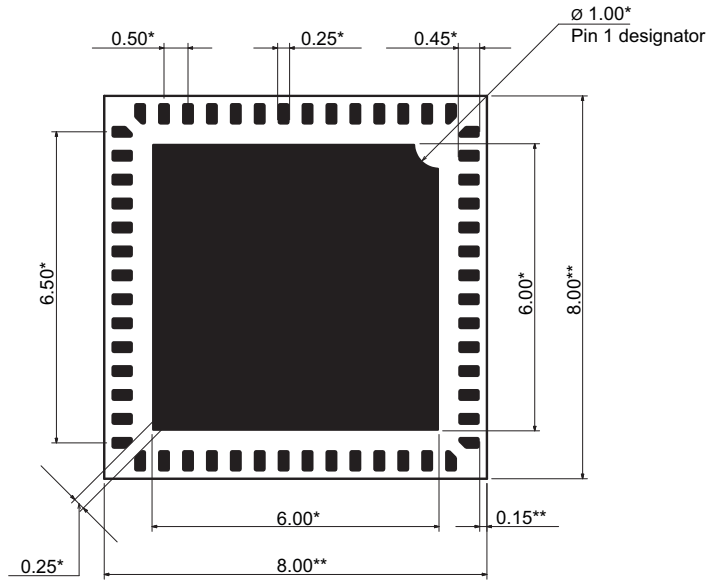
Designation	Value	Conditions
Type	PQFN 56 (MLPQ)	56 pins (+GND plane)
Grid	0.5 mm	
Dimensions	8 x 8 x 1.1 mm	→ see 'dimensional diagram'
Pin surface plating	Au	Cu, Au flash plating
Moisture sensitive level (MSL)	Level 3	acc. to JEDEC J-STD-020D, → see 'Moisture sensitivity' in chapter Processing

Table 6: Package specifications

Dimensional diagram



Side view



Bottom view

* Tolerances ± 0.05 mm, defined by PCB substrate
** Tolerances ± 0.1 mm, related to package outline
All measurements in mm

0909b

Illustration 1: PQFN measuring

3 Processing

PCB plating It is recommended to use chemical NiAu plating.

PCB footprint The following PCB footprint is recommended for engineering samples:

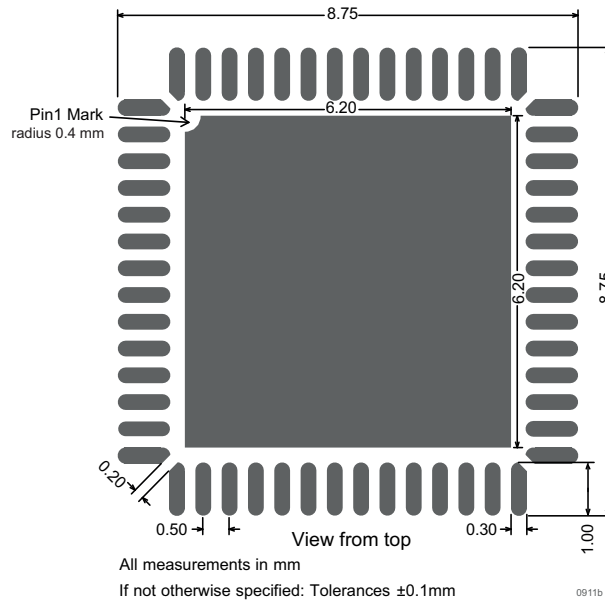


Illustration 2: PCB footprint for engineering samples

The following PCB footprint is recommended for series production:

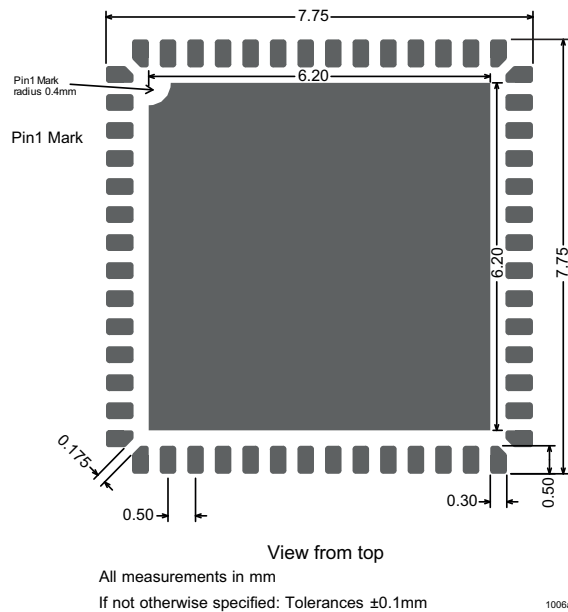
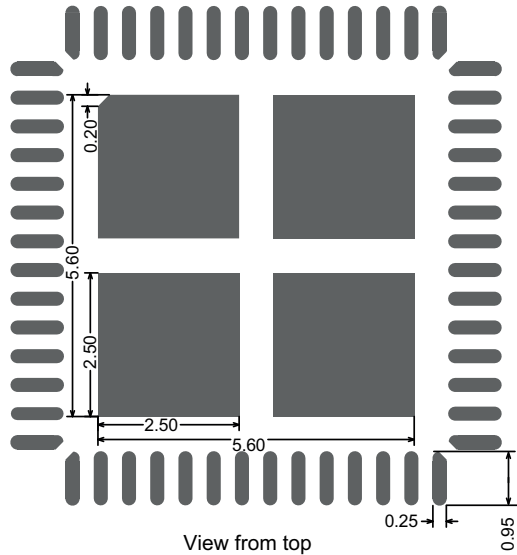


Illustration 3: PCB footprint for series production

Solder Mask clearance A clearance of 60-75 μm is recommended between the copper land and the solder mask.

Solder paste stencil design The following stencil design is recommended for applying the solder paste in engineering samples:



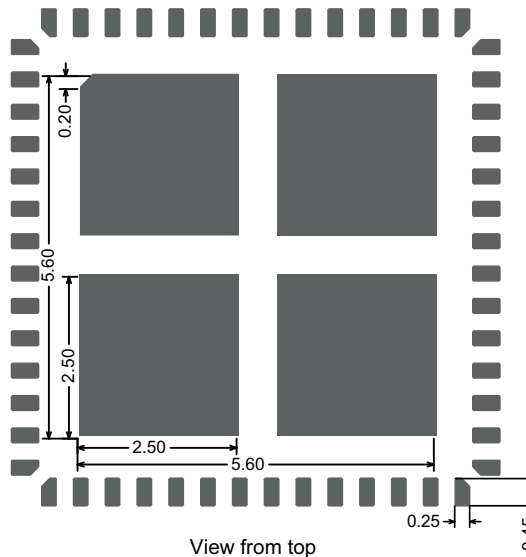
All measurements in mm

If not otherwise specified: Tolerances $\pm 0.1\text{mm}$

0912c

Illustration 4: Solder paste measuring for engineering samples

The following stencil design is recommended for applying the solder paste in series production:



All measurements in mm

If not otherwise specified: Tolerances $\pm 0.1\text{mm}$

1007a

Illustration 5: Solder paste measuring for series paste

Soldering conditions The following RoHS compliant soldering conditions are recommended:

- Soldering conditions: IPC/JEDEC J-STD-020D
- Solder paste: Lead-free, recommended: ALPHA® OM-338-T
- PCB surface plating: Chem. NiAu
- Soldering profile:

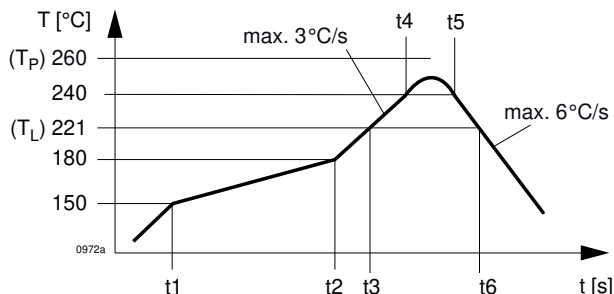


Illustration 6: Soldering profile

	Temperature [$^{\circ}\text{C}$]	Phase	Time [s]	
			Typ.	Max.
Preheating	150...180	t1...t2	40	120
Heating (liquidus, T_L)	> 220	t3...t6	45	60
Soldering	240...250	t4...t5		3
Max. temperature (T_P)	< 260	-	-	

Table 7: Soldering profile

Moisture



NOTICE

Moisture can cause damage to the Security Module

The Security Module package is sensitive to moisture. Moisture trapped inside the package can expand during the reflow soldering process and thus damage the package.

» Process the SM within the time frame given on the bag label (2a).


	<p>CAUTION This bag contains MOISTURE SENSITIVE DEVICES</p>	<p>LEVEL</p>	<p>Level defined by IPC/ JEDEC Standard J-STD-020</p>
		<p>3</p>	
<p>1. Shelf live in sealed bag: 12 month at < 40 °C and < 90 % RH 2. After this bag is opened, devices that will be subject to infrared reflow, vapour-phase reflow or equivalent processing must be: a) Mounted within 150 hours at factory conditions of ≤ 30 °C / 60 % RH b) Stored at ≤ 10 % RH 3. Devices require baking, before mounting, if: a) Humidity Indicator Card is >10 % RH when read at 23 ±5 °C b) Conditions 2a or 2b are not met 4. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure</p>			
			<p>Bag Seal Date</p> <p>12.10.2010</p>

Illustration 7: MSL label

Reference conditions for drying mounted or unmounted SMD packages
(user bake: floor life begins counting at time = 0 after bake)

Level	Bake @ 125 °C +10/-0 °C < 5% RH		Bake @ 90 °C +8/-0 °C < 5% RH		Bake @ 40 °C +5/-0 °C < 5% RH	
	Exceeding Floor Life by > 72 h	Exceeding Floor Life by < 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by < 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by < 72 h
3	8 hours	6 hours	25 hours	20 hours	8 days	7 days

Table 8: Bake parameter

Ultrasonic cleaning



NOTICE

Ultrasonic cleaning can cause damage to the incorporated crystals

» Ultrasonic cleaning is not recommended.

ESD protection



NOTICE

Danger to electronical components caused by electrostatic discharge

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

» Handle integrated circuits with appropriate precautions to avoid ESD damage.

4 Appendix

ESD guideline



Please observe the following ESD protection regulations (ESD = Electro- Static Discharge) when handling the microchips:

Handling components The reader chip has to be kept in the closed original ESD protective packaging at all times when in storage and during transportation. Components may only be removed from the ESD protective packaging in workplaces which are designed for such activities and which are ESD secure. Do not remove the components until you are at the exact location where they will be processed. Components may only be removed from the ESD protective packaging by persons familiar with and observing both the general and the ESD regulations described here.

Ambient conditions To avoid static electricity discharge (ESD) while working, comply with the following regulations:

General:

- Designate ESD secure zones
- Post the ESD regulations
- Check the ESD protective regulations periodically (electrical conductivity)
- Designate grounded discharge surfaces at the entrance of ESD zones for people who enter
- Ensure sufficient relative humidity (min. 45 %)
- Use only anti-static clear plastic binders (for work papers)
- Instruct participating employees
- Inform non-participating employees
- Ensure that all employees and visitors comply with the regulations

Workplace:

- Electrically-conductive work substrate grounded
- Electrically-conductive wristband grounded
- Electrically-conductive work chair
- Electrically-conductive flooring grounded
- Grounded machines and furniture
- Connect all work equipment mentioned above to the same ground potential

Employees:

- Always wear (contact with skin) and ground wristband when working
- Wear electrically-conductive work coat
- Wear electrically-conductive shoes or discharging contact strips
- Work with ESD components in ESD secure workplaces only

SM-6x00 delivery forms The following delivery forms are available:

Option 1: Tape and Reel

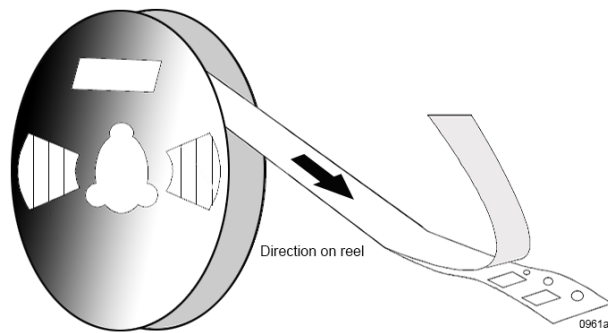


Illustration 8: Tape and Reel

Parts per reel 200 or 500 pcs
 Reel diameter 7"
 Carrier width 16 mm
 Carrier pitch 12 mm

Option 2: Cut Tape

Quantity 10 ... 199 pcs
 Without leader / trailer → see section "Tape leader and trailer dimensions" below

Tape leader and trailer dimensions

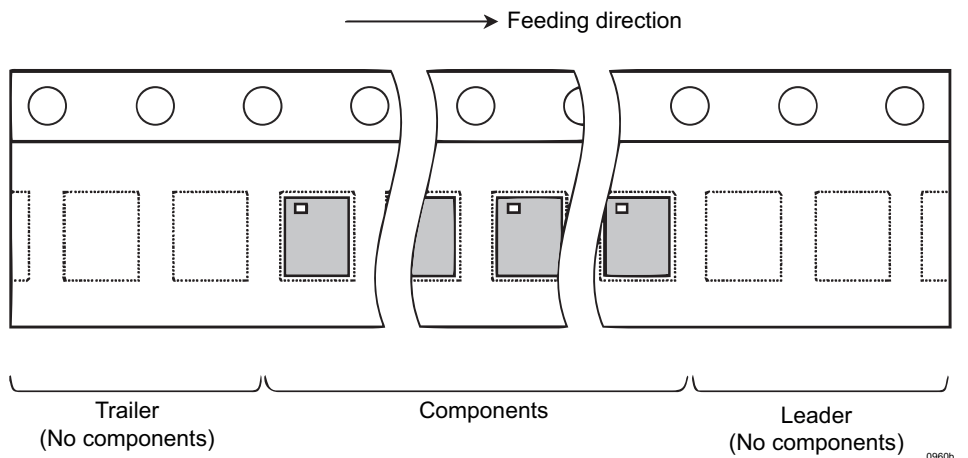


Illustration 9: Carrier tape

	Tape and Reel	Cut Tape
Trailer	160 mm min.	0 mm
Leader	400 mm min.	0 mm

Table 9: Dimensions depending on delivery form

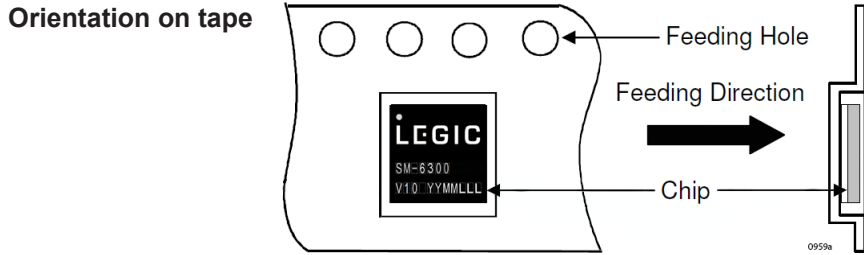


Illustration 10: Orientation on carrier tape

Packing Cardboard box

4.1 RoHS Declaration

LEGIC Identsystems Ltd
 Binzackerstrasse 41
 CH-8620 Wetzikon, Switzerland

declares herewith that the products mentioned above are in compliance with directive 2011/65/EU of the European Parliament and of the council of 8th June 2011 on the 'Restriction of the use of certain hazardous substances in electrical and electronic equipment - (RoHS Directive)'.

Smartcard ICs		
LEGIC prime	MIM256-MN	Wafer
LEGIC prime	MIM1024-MN	Wafer
LEGIC advant	ATC1024-MV110	Wafer
LEGIC advant	ATC4096-MP311	Wafer / MOA4 Module
LEGIC advant	ATC4096-MP312	Wafer / MOB6 Module
LEGIC advant	CTC4096-MP410	Wafer
LEGIC advant	CTC4096-MM410	Wafer
Reader ICs		
All 6000 series reader ICs		
All 6100 series secure element ICs		

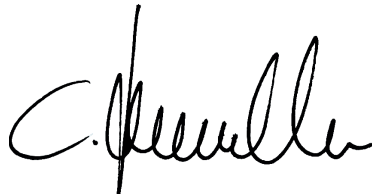
These hazardous substances are:

- Mercury
- Lead **
- Cadmium
- Hexavalent chromium
- Polybrominated biphenols (PBB)
- Polybrominated diphenol ethers (PBDE)
- Di (2-ethylhexyl) phthalate (DEHP) *
- Butyl benzyl phthalate (BBP) *
- Diethylhexyl phthalate (DEHP) *
- Diisobutyl phthalate (DIBP) *

Legend: * In accordance with amendment under Commission Delegated Directive (EU) 2015/863

** Exemption 7c-I

Wetzikon, 29th January 2021



Christoph Beckenbauer
General Manager



ppa Marcel Piüss
Vice President Innovation & Technology